Title: METHOD FOR FORMING CONTACT

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Field of Invention

[0001] The present invention relates to a method for forming contacts, and particularly, relates to a method for forming memory contacts on a semiconductor device.

Background of the Invention

[0002] Most integrated circuits are manufactured by repeating several semiconductor processes, e.g. photolithographing, etching, depositing and doping, and are accomplished with many layers. To transmit signals among those layers, contacts and conductive lines are indispensable to modern semiconductor processes, especially for manufacturing memory chips. The contacts in a memory at least include bit-line contacts and gate contacts, and their manufacturing quality has great effect upon functions of the memory.

[0003] Figs. 1~4 show the steps for forming contacts on a semiconductor device in the prior art. The contacts are positioned on a substrate 102 which has a bit-line contact area 100 and a gate contact area 200. Fig. 1A shows the bit-line contact area 100 which includes a first polysilicon layer 104, a conductive layer 106, a first dielectric layer 108, a side wall 110, a second dielectric layer 112, a third dielectric layer 114, a fourth dielectric layer 116 and a second polysilicon layer 118. Fig. 1B shows the gate contact area 200 which includes a third polysilicon layer 204, the conductive layer 106, a fifth dielectric layer 208, the fourth dielectric layer 116 and the second polysilicon layer 118.

[0004] Referring to Fig. 1A and Fig. 1B, the method of the prior art coats a photoresist 120 on the bit-line contact area 100 as well as the gate contact area 200, and then etches the two areas. Hence, a bit-line contact is formed on the bit-line contact area 100 as Fig.

2A shows; however, a gate contact is not formed yet insofar as Fig. 2B shows. The method of the prior art needs further steps of coating another photoresist 210 on the gate contact area 200, as Fig. 3A shows, and then etching the fifth dielectric layer 208 to form the gate contact as Fig. 3B shows.

[0005] This kind of semiconductor process causes the aspect ratio too small to facilitate photoresist removal.

Summary of the Invention

[0006] The present invention provides a method for forming contacts on a semiconductor device, especially for forming memory contacts. The contacts mentioned herein are positioned on a substrate having a bit-line contact area and a gate contact area.

[0007] The method of the present invention includes the steps of forming an opening on the gate contact area, depositing a dielectric layer on the bit-line contact area and the opening, coating a photoresist to define a bit-line contact opening on the bit-line contact area and a gate contact opening on the gate contact area, etching the dielectric layer while using the photoresist as a mask to form the bit-line contact opening and the gate contact opening, removing the photoresist, and forming a conductive layer on the bit-line contact opening and the gate contact opening.

Brief Description of the Drawings

[0008] Fig. 1A illustrates a sectional view of the bit-line contact area in the prior art;

[0009] Fig. 1B illustrates a sectional view of the gate contact area in the prior art;

[0010] Fig. 2A and Fig. 2B illustrate sectional views for forming the bit-line contact opening in the prior art;

[0011] Fig. 3A and Fig. 3B illustrate sectional views for forming the gate contact opening in the prior art;

[0012] Fig. 4A illustrates a sectional view of the bit-line contact area of the present invention;

[0013] Fig. 4B illustrates a sectional view of the gate contact area of the present invention;

[0014] Fig. 5A and Fig. 5B illustrate sectional views for coating a photoresist to form an opening of the present invention;

[0015] Fig. 6A and Fig. 6B illustrate sectional views after the photoresist is removed;

[0016] Fig. 7A and Fig. 7B illustrate sectional views for depositing a dielectric layer;

[0017] Fig. 8A and Fig. 8B illustrate sectional views for coating another photoresist; and

[0018] Fig. 9A and Fig. 9B illustrate sectional views for forming the bit-line contact and the gate contact.

Detailed Description

[0019] Figs. 4~ 9 show an embodiment of the present invention. Fig. 4A shows the structure of a bit-line contact area 100 which includes a first polysilicon layer 104, a conductive layer 106, a first dielectric layer 108, a side wall 110 and a second dielectric layer 112. Fig. 4B shows the structure of a gate contact area 200 which includes a third polysilicon layer 204, the conductive layer 106 and a fifth dielectric layer 208.

[0020] The method of the present invention includes the step of forming an opening on the gate contact area 200. As Fig. 5A and Fig. 5B show, the method coats a photoresist 122 on the bit-line contact area 100 and the gate contact area 200 to define an opening pattern on the gate contact area 200 by means of the photolithography technique of the prior art. Next, the method etches the fifth dielectric layer 208 and then removes the

photoresist 122. As Fig. 6A shows, the structure of the bit-line contact area 100 does not change, but as Fig. 6B shows, the gate contact area 200 forms an opening 210.

[0021] Then the method deposits a dielectric layer on the bit-line contact area 100 and the opening 210. As Fig. 7A and Fig. 7B show, the dielectric layer includes a third dielectric layer 114 and a fourth dielectric layer 116. In the embodiment, the third dielectric layer 114 is a borophospho-silicate glass (BPSG) layer. It is noted that an annealing process is preferably executed after the borophospho-silicate glass layer is deposited in order to reduce resistivity. The annealing temperature is 850~950℃ and the deposition depth of the borophospho-silicate glass layer on the bit-line contact area 100 after annealing is 2400~2500Å. Moreover, the fourth dielectric layer 116 of the embodiment is a tetraethyl orthosilicate (TEOS) layer of a depth of 2600~4500 Å.

[0022] The method of the present invention further includes the step of forming a polysilicon layer 118 as a hard mask when etching the third dielectric layer 114 and the fourth dielectric layer 116.

[0023] Referring to Fig. 8A and Fig. 8B, the method of the present invention coats another photoresist 124 to define a bit-line contact opening 126 on the bit-line contact area 100 and a gate contact opening 212 on the gate contact area 200.

[0024] Then the third dielectric layer 114 and the fourth dielectric layer 116 is etched by using the photoresist as a mask to form the bit-line contact opening 126 and the gate contact opening 212. Next, the method removes the photoresist 124 so that the bit-line contact opening 126 and the gate contact opening 212 are accomplished as Fig. 9A and Fig. 9B show. Finally, a conductive layer is formed on the bit-line contact opening 126 and the gate contact opening 212 to be a medium for signal transmission.

[0025] The width W of the bit-line contact opening 126 made by the method of the present invention is 60~70nm, which is 50~75% wider than that of the prior art. The larger aspect ratio facilitates photoresist removal.

[0026] The above description of the preferred embodiments is expected to clearly expound the characteristics of the present invention but not expected to restrict the scope of the present invention. Those skilled in the art will readily observe that numerous modifications and alterations of the apparatus may be made while retaining the teaching of the invention. Accordingly, the above disclosure should be construed as limited only by the bounds of the claims.